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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,348	02/28/2002	Tadayoshi Kobori	FUJI 126	5632

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EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,348	KOBORI, TADAYOSHI	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-13,15-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-5, 7-13, 15-17, 19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 10/18/04. Currently claims 1, 3-5, 7-13, 15-17, and 19-20 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. *Claims 1, 3-5, 7-13, 15-17, and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu (US 6219797).*

Regarding claim 1, Liu discloses the central processing unit that operates with one of a first clock and a second clock, the second clock having a shorter period than the first clock (e.g., col. 11, lines 61-67); a clock generating circuit for generating the second clock upon receiving a start signal (e.g., Fig. 3, follow "SWB=1 and external activity occurs" branch); a clock switching circuit for normally supplying the first clock to the central processing unit to cause the central processing unit to operate with the first clock, and for supplying the second clock, instead of the first clock, to the central processing unit to cause the central processing unit to operate with the second clock when a predetermined condition is present (e.g., Fig. 5); and an interrupt control circuit for supplying the start signal to both the central processing unit and the second clock generating circuit when the interrupt control circuit receives an interrupt request signal, the start signal being supplied to the second clock generating circuit without passing

through the central processing circuit, the start signal causing the central processing unit to start preparation for the interruption (e.g., Fig. 5, "interrupt/serial port"; col. 13, lines 31-36), causing the clock generating circuit to start producing the second clock while the central processing unit is starting preparation (e.g., col. 13, lines 31-36).

Regarding claim 3, Liu also discloses the predetermined condition is present when the central processing circuit completes the preparation for the interruption, and oscillation of the second clock derived from the second clock generating circuit becomes stable (e.g., col. 14, lines 55-57).

Regarding claim 4, Liu also discloses wherein the predetermined condition is present when the longer of a time needed for the central processing circuit to complete the preparation for the interruption and a time needed for second clock oscillation to become stable elapses (e.g., col. 13, lines 36-40).

Regarding claim 5, Liu also discloses wherein the central processing unit starts processing interruption data at a high speed upon receiving the second clock (e.g., col. 13, lines 29-33).

Regarding claim 7, Liu also discloses wherein the start signal is supplied in parallel to the central processing unit and the second clock generating circuit (e.g., col. 13, lines 33-36).

Regarding claim 8, Liu discloses the central processing unit adapted to operate with a first clock; a clock generating circuit for generating a second clock upon receiving an interrupt request signal, the second clock having a shorter period than the first clock (e.g., Fig. 5); and an interrupt control circuit for storing interruption data in

accordance with the second clock, and for supplying a start signal to the central processing unit upon receiving the interrupt request signal (e.g., col. 13, lines 33-36), to cause the central processing unit to start preparation of the interruption and feeding the interruption data to the central processing unit after the central processing unit completes the preparation of the interruption such that the central processing data performs the interruption with the interruption data (e.g., col. 13, lines 36-42), with interruption performed in accordance with the first clock (e.g., col. 14, lines 25-26).

Regarding claim 9, Liu also discloses wherein the interrupt control circuit stores the interruption data after supplying the start signal to the central processing unit (e.g., col. 13, lines 36-42).

Regarding claim 10, Liu also discloses the interrupt request signal is supplied to the clock generating circuit without passing through the interrupt control circuit (e.g., col. 13, lines 36-42).

Regarding claim 11, Liu also discloses wherein the second clock has a short period sufficient not to cause an overflow of the interruption data (e.g., col. 13, lines 33-36, 40-42).

Regarding claim 12, Liu also discloses wherein the clock generating circuit and the interrupt control circuit receive the interrupt request signal at substantially the same time (e.g., col. 13, lines 29-33).

Regarding claim 13, Liu also discloses the interrupt control circuit stores the interruption data after oscillation of the second clock produced from the clock generating circuit becomes stable (e.g., col. 13, lines 36-40).

Regarding claim 14, Liu also discloses the central processing circuit performs the interruption in accordance with the first clock (e.g., col. 13, lines 7-17).

Regarding claim 15, Liu also discloses wherein the preparation of the interruption and generation of the second clock are initiated at substantially the same time (e.g., col. 13, lines 29-33).

Regarding claim 16, Liu also discloses the start signal is supplied to the central processing unit at substantially the same time the interrupt request signal is supplied to the clock generating circuit (e.g., col. 13, lines 29-33).

Regarding claim 17, Liu discloses central processing means adapted to operate with one of a first clock and a second clock, the second clock having a shorter period than the first clock; means for generating the second clock upon receiving a start signal; means for normally supplying the first clock to the central processing means to cause the central processing means to operate with the first clock, and for supplying the second clock, instead of the first clock, to the central processing means to cause the central processing means to operate with the second clock when a predetermined condition is present (e.g., Fig. 5); and means for supplying the start signal in parallel to both the central processing means and the second clock generating means upon receiving an interrupt request signal, the start signal causing the central processing means to start preparation for the interruption (e.g., col. 13, lines 31-42) , causing the clock generating circuit to start producing the second clock while the central processing unit is starting preparation (e.g., col. 13, lines 31-36).

Regarding claim 19, Liu discloses central processing means adapted to operate with a first clock; means for generating a second clock upon receiving an interrupt request signal, the second clock having a shorter period than the first clock; means for storing interruption data in accordance with the second clock (e.g., Fig. 5); means for supplying a start signal to the central processing means upon receiving the interrupt request signal, to cause the central processing means to start preparation of the interruption (e.g., col. 13, lines 38-42); and means for feeding the interruption data to the central processing means after the central processing means completes the preparation of the interruption such that the central processing means performs the interruption with the interruption data in accordance with the first clock (e.g., col. 13, lines 19-28; col. 14, lines 25-26).

Regarding claim 20, Liu also discloses the means for storing the interruption data stores the interruption data after the means for supplying the start signal supplies the start signal to the central processing means (e.g., col. 13, lines 38-42).

Response to Arguments

Applicant's arguments filed 10/18/04 have been fully considered but they are not persuasive.

Regarding claims 1 and 17, Applicant argues that amended claim distinguishes from Liu in that "a start signal is supplied to both a CPU and to a second clock generating circuit substantially simultaneously" (p. 8); however, as can be seen from, for example, Figure 5, the start signal to the CPU emanates from the "Clock Generator"

which is derived directly from the interrupt detection (e.g., Fig. 5, "86:Set Default State") and is considered the start of preparation for the interruption.

Regarding claims 8 and 19, Applicant argues that "[a]lthough Liu may change clock speeds during an interrupt, the reference neither discloses nor suggests using first and second clock signals" (p. 8); however, it is seen that Liu in fact teaches switching to the first clock speed to process the interrupt once the data input, received at the second clock speed, has completed. An exemplary passage (col. 14, lines 25-26), is cited supra regarding claim 8 in order to clarify this.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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